## **REMARKS/ARGUMENTS**

Applicants representative would like to thank Examiner Vartanian for taking the time to conduct a telephonic interview to discuss the remaining issues in this case. As noted in the interview summary, the claims were discussed in light of U.S. Patent No. 4,584,695 to *Wong et al*, and U.S. Patent No. 4,975,634 to *Shohet*, but an agreement was not reached on the allowability of the claims over *Shohet*.

Further comparison of *Shohet* with the pending claims reveals that the reference neither teaches nor suggests all the elements of the claims. Accordingly, reconsideration and withdrawal of the rejection of claims 1–2, 5, 7–11, and 16 under 35 U.S.C. § 102(b), and claims 6, 15, 17, and 19–23 under § 35 U.S.C. § 103(a) over *Shohet* is respectfully requested in light of the following remarks.

Claim 1 includes a method of measuring jitter in a digital signal where an offset reference clock signal is formed that is "offset by a predetermined frequency amount from said digital signal." See claim 1, lines 2–3. Similarly, claims 10 and 15 include a means and an offset unit, respectively, which form an offset reference clock signal that is offset by a predetermined frequency amount from the digital signal. See claims 10 and 15, lines 3–4. As the specification notes, "[t]he effect of the offset of the reference clock signal is that the sampling point is not fixed relative to the transition point over the bits of the input signal, but instead moves relative thereto." See Specification, page 2, line 26 to page 3, line 3. The present invention takes advantage of the relative motion of the offset reference clock signal and the input (i.e., digital) signal to scan the pulses in the pulse-train of the digital signal. See, e.g., Specification, page 10, lines 8–25.

In contrast, *Shohet* does just the opposite by making sure the reference clock signal and digital signal are frequency synchronized during a jitter measurement. The jitter measurement device in *Shohet* includes a range adjusting circuit that includes gang switches to insure any adjustment in clock signal frequency is matched in the jittered clock (*i.e.*, digital) signal frequency:

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A range adjusting circuit 20, to be explained more fully below, adjusts the frequency of the high frequency clock signal  $f_{Ho}$  from terminal 14 and the jittered clock signal  $f_{Jo}$  from terminal 16. The adjustment is illustrated as a pair of gang switches such that the adjustment of the high frequency clock  $f_H$  and the jittered clock signal  $f_{Jo}$  are both adjusted by the similar amount to produce signals  $f_H$  and  $f_J$ .

Shohet, Col. 2, lines 57-64.

Shohet does describe the ability to adjust the relative phase of the two clock signals, but a phase adjustment is not the same thing as a frequency offset. Shohet, Col. 3, lines 50–56. Adjusting the phase of the reference clock signal relative to the jittered clock signal does not change the frequency of either signal. After a phase adjustment, the reference clock and jittered clock signals remain fixed with respect to each other (except for jitter) during the jitter measurement. There is no description or suggestion in Shohet that frequencies be adjusted (i.e., offset) so that the reference clock signal moves over the jittered clock signal during a jitter measurement. If anything, Shohet teaches away from having the reference signal moving relative to the jittered clock signal during the measurement, because this movement would be read as a jitter measurement by the measurement device. Shohet Col. 3, lines 31–34.

Shohet neither describes nor suggests all the elements of claims 1, 10, and 15, and these claims are allowable over the reference. For at least the same reason, claims 2–3, 5–9, 11–12, and 16–23, which depend from claims 1, 10 and 15, respectively, are also allowable over Shohet. Accordingly, withdrawal of the rejection of claims 1–2, 5, 7–11, and 16 under 35 U.S.C. § 102(b), and claims 6, 15, 17, and 19–23 under § 35 U.S.C. § 103(a) over Shohet is respectfully requested.

## CONCLUSION

Formal drawings have been provided with this Response that correct the informalities in Figs. 4–7. In view of the submission of formal drawings and the remarks above, Applicants believe pending claims 1–3, 5–12, and 15–23, are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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TOWNSEND and TOWNSEND and CREW LLP

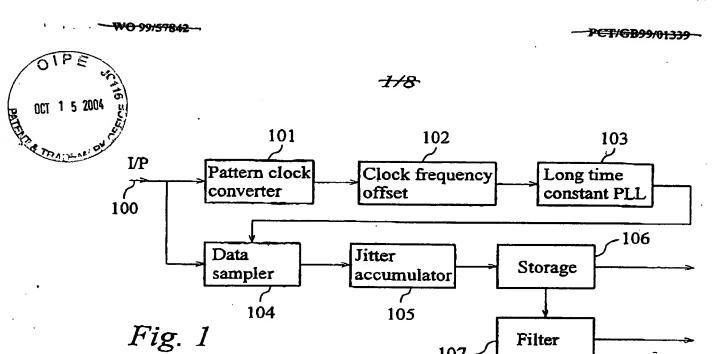
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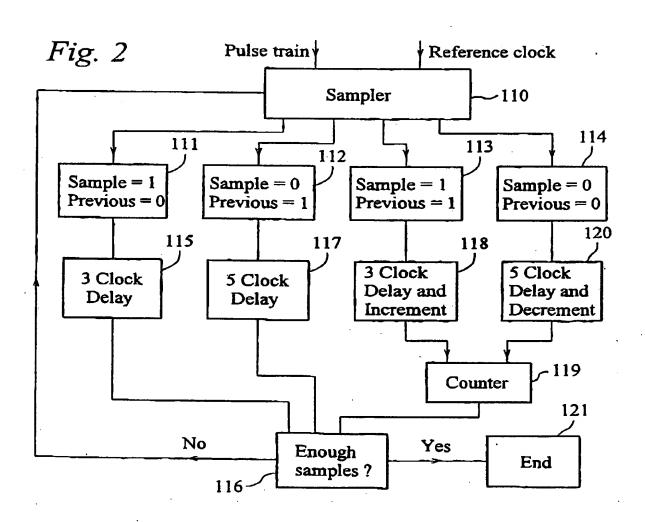
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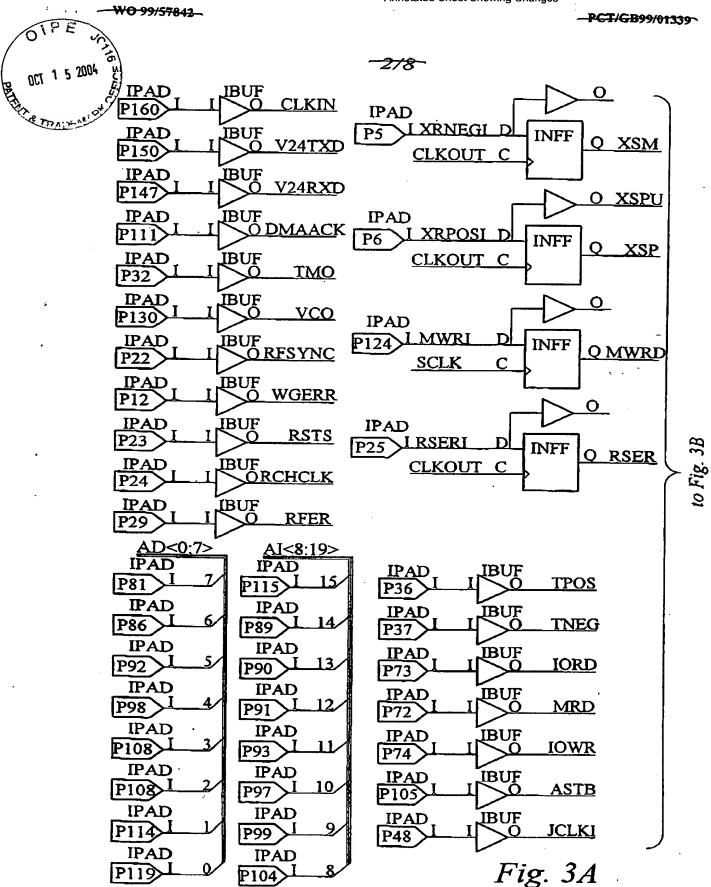
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<del>-3/8</del>-10 -- 11 CLKOUT CLKOUT CLKIN CLKIN CLKOUT CLKOUT TXBRTS TXBRTS TXCKEN TXBERT **TXBERT** TXCKEN CLOCKGEN TMO TMO TXTSSEL CLKOUT CLKOUT RXCKEN RXCKEN CLKOUT CLKOUT **XTPOS XTPOS** XSM SM RDLCLK RDLCLK TXBRTS TXBRTS SP **RPOS XRPOS** XSP TXBERT TXBERT GETCLOCK RNEG XRNEG **INJERR TXPRBS** INJERR CLKOUT CLKOUT WGCLK WGCLK CLKOUT CLKOUT **XTPOS XTPOS** RXCKENIRXCKEN TXCKEN XTNEG XTNEG TXCKEN RESYNC RESYNC TXPDAT TXPDAT TSSEL **TPOS** TPOS RFER CRCERR CRCERR RFER TNEG TNEG RESYNC RFSYNC FASERR FASERR TDLCLK TDLCLK TXHDB3 RCHCLK RCHCLK **TXBERT** RSTS RSTS G703ERRS RX BERT CLKOUT CLKOUT **TXCKEN TXCKEN** DOJT TDLCLKTDLCLK TILOG CLKOUT CLKOUT OFFCLK OFFCLK **JMOD1** TMOD1 TJINEN TJINEN RXCKENTRXCKEN **TXCLKGEN** CLOCKOFF D<0:7> D<0:7> DOJIT DOJIT VCO SIGIN SIGIN COMP

from Fig. **VCO JCLKI** COMP JCLKI SCLK PLLSTUFF **SCLK** SCLK XSPU XSPU

COUNT COUNT UP EICLK EICLK TWO TWO JITDET SCLK

SCLK

COUNT SMP<0:7>|SMP<0:7> STOPPED STOPPED JITCOUNT D<0:7> SCLK D<0:7> E1CLK **DMARO** E1CLK **DMARO** 

DMAACK DMAACK MXADDR MXADDR

STOPPED STOPPED MNADDR MNADDR MWRD MWRD SMP<0:7> SMP<0:7> JITOUT JITTER

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CLKOUT CLKOUT JMOD1 JMOD1 JQ<0:2> JQ<0:2>

ЛТАМР ПТАМР TJINEN TINEN **TXJITGEN** <u>13</u> TX JITTER

CLKOUT STOPPED STOPPED CLKOUT **ASTB** astb JQ<0:2> JO<0:2 INJERR **IOWR** OWR INJERR **IORD** IORD MRD MRD IOEN IOEN MXADDR MXADDR D<0:7> D<0:7 DMAACK DMAACK

AD<0:7> ЛТАМР AD<0:7> ЛТАМР AI<8:15> AI<8:15> RECONEN RECONEN MNADDR MNADDR TWO TWO **GLUE V40** 

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Fig. 3B

30 to Fig. OIPE

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DMARQ OPAD	TDLCLK I OBUF OPAD OPAD P35
COMP O P131	RSER I OBUF WGDATA O P121
SIGIN O P129	V24TXD I OBUF OPAD OPAD P152
XRPOS O OPAD P27	V24RXD I OBUF O OPAD OPAD OP15
XRNEG OPAD P28	TXCKEN I OBUF O TXCLK O P13
WGCLK O P88	WGERR I OBUF O PAD O P68
FASERR OPAD	TXPDAT I OBUF O P33
CRCERR O P64	RDLCLK I OBUF OPAD OPAD OPAD
IOEN O P113	OBUF O Plo3
RECONEN O P76	OBUF OPAD O P137
$\begin{array}{cc} XTPOS & O \\ \hline P15 \end{array}$	OBUF OPAD OP154
XTNEG OPAD P14	JCLKI I OBUF OPAD OPAD P54
OFFCLK O P45	JITTER

Fig. 3C

